TMC22061

Demonstration Board for the TMC22091 Digital Video Encoder

CCIR-601 Input

Features

- Parallel CCIR601-Format ECL Input
- Multiple Video Formats
  NTSC
  NTSC-EIA
  PAL
  PAL-M
- Composite and S-Video Outputs
- Built-In Test Patterns
  Color Bars
  Modulated Ramp
- No External Components Required

Applications

- Evaluation of TMC22x91 Digital Encoders
- System Breadboarding
- Encoder Control Program Development

Related Products

- TMC22091/TMC22191 Digital Video Encoders
- TMC22290/TMC22291 Digital Video Encoders

Description

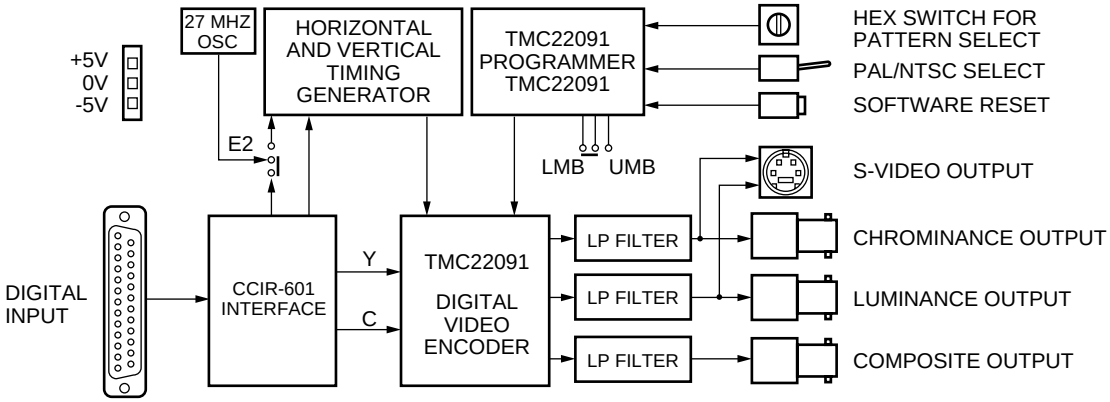
The TMC22061P7C encoder demonstration board converts 8-bit parallel digital component video, (CCIR Rec. 656 or SMPTE RP 125, a.k.a. "601") into analog composite video using the TMC22091 digital video encoder. The board supports multiple standards, operating in PAL, PAL-M, NTSC, and NTSC-EIA (zero setup) television formats.

A 27 MHz crystal oscillator is provided for cases where a CCIR-601 source is not available. When operated from the on-board oscillator, only the internally generated color bars and modulated ramp can be produced.

The TMC22061 is designed to demonstrate the performance of the TMC22x91 family of Digital Video Encoders, while providing a convenient testbed for developing specific programming for the encoder and evaluating the resulting waveforms. It also offers an example of design practices that result in high-quality video performance.

The board supports multiple standards, operating in PAL, PAL-M, NTSC, and NTSC-EIA (zero setup) television formats. The data must be provided with the proper frame rate, but any supported 50Hz format may be produced with the supplied programs.

Block Diagram



The board accepts 8-bit parallel digital component video, (CCIR Rec. 656 or SMPTE RP 125, a.k.a. "601") at a standard D25 connector in differential ECL format, translates the data to TTL format, strips the Timing Reference Signal from the datastream to generate H&V Sync, and passes the digital video stream to the Encoder in a 16-bit 13.5 MHz format.

A simple EPROM-based programmer is provided, which downloads the selected configuration (one of 64) to the Encoder when the reset button is pressed. This EPROM holds both control register data and Color-Look-Up-Table (CLUT) patterns in 1K blocks. Sixteen pages are selected by a rotary switch, and additional switches are provided for selecting among the four 16K banks.

A 27 MHz crystal oscillator is provided for cases where a CCIR-601 source is not available. When operated from the on-board oscillator, only the internally generated color bars and modulated ramp can be produced.

The board operates from standard ±5V supplies. When used in stand-alone mode, only +5V is required.

CCIR-601 Interface

The CCIR-601 data stream is terminated into differential ECL-to-TTL converters. The translated data is latched through U23 at a 27 MHz rate and then passed to a YC demultiplexer. Here, the luminance and chrominance data words are separated into two data streams termed Y and C, respectively. This YC data goes directly into the TMC22091, which separates the C data stream into its two color difference signals and interpolates them to the same sample rate as Y data. This interpolation improves the horizontal color definition.

The TRS decoder extracts the field (F), vertical blanking (V), and horizontal blanking (H) information from the 601 data stream for use in the timing signal generation on the board. The TRS decoder also produces the pixel counter reset and the LDV signal for latching the YC data into the TMC22091.

Horizontal and Vertical Timing

The pixel counter (U4, U5, and U1) is decoded to produce the VHSYNC\ and PDC signals required by the TMC22091 for horizontal synchronization. A 2x line rate clock, H/2_CLK, used in the VVSYNC\ generation, is also produced along with P_CLOCK and DATA_EN. P_CLOCK is used to clock the program counters and the DATA_EN signal used in the YC demultiplexing circuit.

A 4-bit counter embedded in U9 is started whenever V goes HIGH, which occurs at the beginning of each vertical blanking interval. This counter is clocked by H/2_CLK, which enables the VVSYNC\ pulse to be produced at the same time as the first vertical sync pulse in each field. The PGM output signal ensures that the software reset signal, RES_OUT, goes HIGH 15 half-line periods before the program counter starts.

Software Reset

A software reset occurs whenever the pushbutton switch, S3, is depressed. The software reset is latched through U9 to ensure a known relationship between the internal pixel clock of the TMC22091 and the externally generated LDV, PDC, VHSYNC\, and VVSYNC\ signals. When S3 is depressed the internal state machines of the TMC22091 are reset and the outputs are disabled. When S3 is released the program counter is started at the beginning of the next vertical blanking period. Software Reset is required after power-up and after each functional change.

Programming the TMC22091

A 12-bit counter (U6, U7, and U8) is used to produce the addresses used in programming the TMC22091. U11 produces the required R/W\, A1:0, and CS\ signals, while U12 contains 32 different pages of setup data for NTSC and another 32 pages for PAL (selected via switch S2). Switch S1 selects between different flavors of NTSC and PAL operation. To ensure that the outputs of the programmable logic are correctly timed to transitions on the microprocessors data bus, they are addressed at four times the rate that U12 is addressed. The 16 pages of setup data are selected by the rotary switch S1, as shown in Table 1.

Table 1. Board Operational Setups

Rotary Switch Position	Board Function
0	Color bars test signal (8-bars)
1	Color bars test signal (9-bars)
2	Modulated ramp test signal
3	Encodes CCIR-601 input data (normal operation)
4	Subcarrier data limited to 28-bit resolution
5	Subcarrier data limited to 24-bit resolution
6	Luminance data limited to 6-bit resolution
7	Chrominance data limited to 6-bit resolution
8	Luminance and chrominance data limited to 6-bit resolution
9	Inverted luminance data
A	Inverted luminance data and 180° phase shift to chrominance
B	Chrominance data set to constant value in UV CLUTs
C	Color burst phase advanced 10°
D	Color burst phase retarded 10°
E	Reduced active video line length
F	Black burst (NTSC includes pedestal)

The programming of the encoder operation into each of the 64 memory pages by banks of 16 by video standard (*Table 2*) is entirely arbitrary: one could as easily assign CCIR-601 operation in the four supported formats to pages 0-3, and color bars to pages 4-7. The user is encouraged to replace the EPROM with one programmed with other formats of interest.

On-Board Read-Only Memory

Table 3 shows the content format of the EPROM that holds the 64 pages of setup data. The encoder register contents are defined in the TMC22x9y Datasheet.

Table 2. Standards Selection

S1	S2	Format	Memory Pages
LMB	NTSC	NTSC	0-15
LMB	PAL	PAL B/I	16-31
UMB	NTSC	NTSC-EIA	32-47
UMB	PAL	PAL-M	48-63

Table 3. EPROM Address Map

Address	Contents
0	
1	CLUT address pointer set to 00h
2	Start of CLUT data
:	V_{n-1}
:	V_n
:	V_{n+1}
769	End of CLUT data
770	Control Register pointer set to 00h
771	Start of Control Register data
:	
:	
851	End of Control Register data
852	Unused locations set to 00h
:	
:	
1023	Unused locations set to 00h

Output Reconstruction Filters

The 2x oversampling of internal digital data before the output D/A converters of the TMC22091 not only reduces the Sin(x)/x high-frequency roll-off but eliminates complicated reconstruction filters. This is particularly important as the frequency response of digital filters is dependent upon the sample rate, while the frequency of the aliased subcarrier component is fixed. The TMC22091 encoder is designed to drive a 75 Ω line, terminated both at the source and at the load (that is, a 37.5 Ω load.) The filters are internally source terminated. Optional load terminations are provided on the board. If these are not required, simply remove the appropriate links behind the BNC connectors (E4, E5, E6).

Operation Without a CCIR-601 Source

Only rotary switch positions 0, 1, and 2 are useful without a CCIR-601 digital video source available. These switch positions produce color bars and a modulated ramp. These test patterns are inserted into the pixel data path after the CLUTs in RGB format and demonstrate 90% of the circuitry of the TMC22091. To provide a PXCK in the absence of a CCIR-601 source, switch E2 to INTernal.

Power Supply Requirements

The TMC22061P7C board requires 1.25 Amps from the +5 Volt power supply and 0.25 Amps from the -5 Volt power supply. The -5 Volt power supply powers ECL logic devices which have relatively good noise immunity. The +5 Volt power supply not only drives TTL logic devices but it also provides the power to the TMC22091. Therefore, it is recommended that a bench power supply be used with the cable lengths kept to a minimum. When operating in stand-alone mode, only the +5 Volt supply is required.

Table 4. TMC22061 Parts List

Item	Qty	Part/Value	Ref. Designator	P/N, Mfg. No.
1	2	Ferrite Beads	L1, L2	2743001112, FAIR-RITE Prod. Corp.
2	3	Inductors, 1.8µH	L3, L5, L7	IMS-2 1.8µH ±5%, Dale
2	3	Inductors, 1.0µH	L4, L6, L8	IMS-2 1.0µH ±5%, Dale
3	33	Ceramic capacitor, 0.1 µF	C3-C5, C9-C14, C17-C20, C22-C39, C41 C43	MD015C104KAB, AVX
4	4	Ceramic capacitor, 0.01 µF	C1, C16, C40, C42	MD015C103KAB, AVX
5	3	Ceramic capacitor, 27 pF	C57, C59, C61	SR151A470JAA, AVX
7	3	Ceramic capacitor, 100 pF	C45, C49, C53	SR151A101JAA, AVX
7	6	Ceramic capacitor, 330 pF	C44, C47, C48, C51, C52, C55	SR133A561JAA, AVX
8	2	Tantalum capacitor, 0.47 µF	C2, C15	TAP474K035SCS, AVX
9	2	Tantalum capacitor, 22 µF	C7, C8	TAP226K035SCS, AVX
10	9	Resistor, 75Ω	R15-R20, R22-R24	RN50C75R0F
11	9	Resistor, 120Ω	R3, R5-R12	RN50D1200F
12	1	Resistor, 412Ω	R14	RN50C4120F
13	1	Resistor, 3.3kΩ	R1, R13, R21	RN50C3301F
14	1	Resistor, 4.7kΩ	R2	RN50D4701F
15	1	Resistor, 47kΩ	R4	RN50D4702F
16	1	SIP resistor, 3.3kΩ	RN1	4308R-101-332, Bourns
16A	1	SIP resistor, 3.3kΩ	RN2	4310R-101-332, Bourns
17	1	1N4148 Silicon Diode	CR1	1N4148
18	1	LT1004 Bandgap Reference	CR2	LT1004-1.2, Linear Technology
18A	2	1N4004 Silicon Diode	CR3, CR4	1N4004, Motorola
19	1	TMC22091 Encoder	U18	TMC22091R0C, Raytheon Semiconductor
20	2	16R8 PAL	U9, U20	TIBPAL16R8-15CN, Texas Inst.
21	2	20R8 PAL	U10, U11	TIBPAL20R8-15CNT, Texas Inst.
22	1	27512 EPROM	U12	TMS27C512-120JL, Texas Inst.
23	3	10125 ECL-TTL Translator	U16, U19, U22	MC10125P, Motorola
24	1	74F08 Quad 2-input AND	U13	MC74F08N, Motorola or equiv.
25	1	74LS74 Dual D-type FF	U14	MC74LS74AN, Motorola or equiv.
26	3	74F163 4-bit counter	U1, U5, U4	MC74F163AN, Motorola or equiv.
27	3	74LS163 4-bit counter	U6, U7, U8	MC74LS163AN, Motorola or equivalent
28	1	74F174 Hex D-type FF	U2	MC74F174AN, Motorola or equiv.
29	2	74F374 Octal D-type FF	U17, U23	MC74F374N, Motorola or equiv.
30	1	74HCT374 Octal D-type	U15	MC74HCT374N, Motorola or equivalent
31	2	74F377 Octal D-type FF	U21, U24	MC74F377N, Motorola or equiv.
32	1	Crystal oscillator	Y1	MXO-55GA-2C-27MHz, CTS-Knight F1100H-27MHz, Fox
33	15	Test points	TP1-TP15	ME151-203-100, Mouser

Table 4. TMC22061 Parts List (continued)

Item	Qty	Part/Value	Ref. Designator	P/N, Mfg. No.
34	4	Shorting block		ME151-8000, Mouser
35	4	Jumpers	E1, E4, E5, E6	NSH-36SB-S1-TR, Robinson-Nugent
36	1	Power Connector	J1	ELM033100, PCD
37	3	BNC connectors	J2, J3, J4	31-5431, Amphenol
38	1	S-VIDEO Connector	J5	749263-1, Amphenol
39	1	25-pin D-connector	P1	617BO25SAJ220, Amphenol
40	2	SPDT switch	E2, E7	090320102, Secma Inc.
41	1	SPDT switch	S2	ATIDG-RA-1, Alco Switch
42	1	SPDT switch	S3	TP11FG-RA-0, Alco Switch
43	1	HEX rotary switch	S1	350134GSV, EECO
44	1	PLCC socket		PLCCB-84-PS-T, Robinson-Nugent
45	1	Oscillator socket		ICA-143-SCO-TG30, Robinson-Nugent
46	2	20-pin DIP socket		ICA-203-S-TG30, Robinson-Nugent
47	2	24-pin DIP socket		ICA-243-S-TG30, Robinson-Nugent
48	1	28-pin DIP socket		ICA-286-S-TG30, Robinson-Nugent
49	1	Universal transistor mount		111-080, BIVAR
50	4	Standoff		1902F, Keystone
51	1	Bare PC Board		40X07140 Rev. B, Raytheon Electronics

PAL Functions Listings

Following are the programmable array logic listings of the devices used on the TMC22061P7C evaluation board. These listings are shown as ABEL_HDL source files. The following brief tutorial refers only to terms used for programming logic used on this board.

Sets

A set is a collection of signals and constants that are operated on as one unit. Any operation applied to a set is applied to each element in the set. For example, in U9,

```
count = [c3,c2,c1,c0]
```

Valid operations used in the TMC22061P7C:

Operator	Example	Description
:=	A := [1,0,1]	registered assignment
!	!A	NOT: ones complement
&	A & B	AND
#	A # B	OR
==	A == B	equal
!=	A != B	not equal
<	A < B	less than
<=	A <= B	less than or equal
>	A > B	greater than
>=	A >= B	greater than or equal

The Basic Elements Of A Source File

Module The module statement names the module and indicates the presence of any dummy variables used.

Title The title statement can be used to give a title or description for the module.

Declarations Declarations associate names with devices, pins, nodes, constants, macros, and sets.

Equations It is possible to use equations, state diagrams, or truth tables to describe logic designs. All programmable devices use equations.

End The end statement terminates the module. Comments begin with double quotation marks, " ", and end with either another double quotation mark or the end of line, whichever comes first.

Code Segment 1. U9 - VVSYNC and Reset Logic

```
Board Reference Designator U9
Module  bd1_u9
Title   'VVSYNC generation and reset control logic'
Declarations
       bd1_u9 device "P16R8';
"inputs"
       clk,v,pn,f                  pin 1,2,3,4;
       s_reset                     pin 7;
"outputs"
       c0,c1,c2,c3                 pin 19,18,17,16;
       fb,vvsync,pgmfb,pgm         pin 15,14,13,12;
"notation"
       count = [c3,c2,c1,c0];
       t = (s reset & !pgmfb) # pgm # (v & s_reset & !pgm & pgmfb);
Equations
       !c0         := c0 & t & (count != 15)
                  # !t;
       !c1         := !c0 & !c1 & t & (count != 15)
                  # c0 & c1 & t (count != 15)
                  # !t;
       !c2         := !c2 & !c0 & t & (count != 15)
                  # !c2 & !c1 & t & (count != 15)
                  # c2 & c1 & c0 & t & (count != 15)
                  # !t;
       !c3         := !c3 & !c0 & t & (count != 15)
                  # !c3 & !c1 & t & (count != 15)
                  # !c3 & !c2 & t & (count != 15)
                  # !t;
       !vvsync     := !fb & pn & ((count >= 3) & (count <= 5))
                  # fb & ((count >= 4) & (count <= 5))
                  # !fb & !pn & (count == 5)
                  # ((count >= 6) & (count <= 7));
       !fb         := (!fb & v) # (f & !v);
       pgmfb       := s_reset;
       !pgm        := (count == 15)
                  # s_reset & pgmfb & !pgm
                  # !s_reset;
End    bd1_u9
```

Code Segment 2. U10 - VHSYNC and Data Control Logic

```
Board Reference Designator U10
Module  bd1_u10
Title   'VHSYNC generation and data control logic'
Declarations
       bd1_u10 device "P20R8';
"inputs"
       a0,a1,a2,a3,a4,a5,a6         pin 2,3,4,5,6,7,8
       a7,a8,a9,a0                  pin 9,10,11,14;
clk,pn  pin 1,23;
"outputs"
       vhsync,pdc,hclk              pin 22,21,20;
       h2clk,den,pclk               pin 19,18,17;
       fb                           pin 16;
"notation"
       addr = [a10..a0];
Equations
       !vhsync    := ((addr >= 16) & (addr <= 256));
       !hclk      := ((addr >= 1712) & (addr <= 16));
       h2clk      := ((addr >= 15) & (addr < 256))
                  # !fb;
       !den       := a0;
       !pclk      := !a0;
       !fb        := ((addr >=766) & (addr < 1015);
End
```

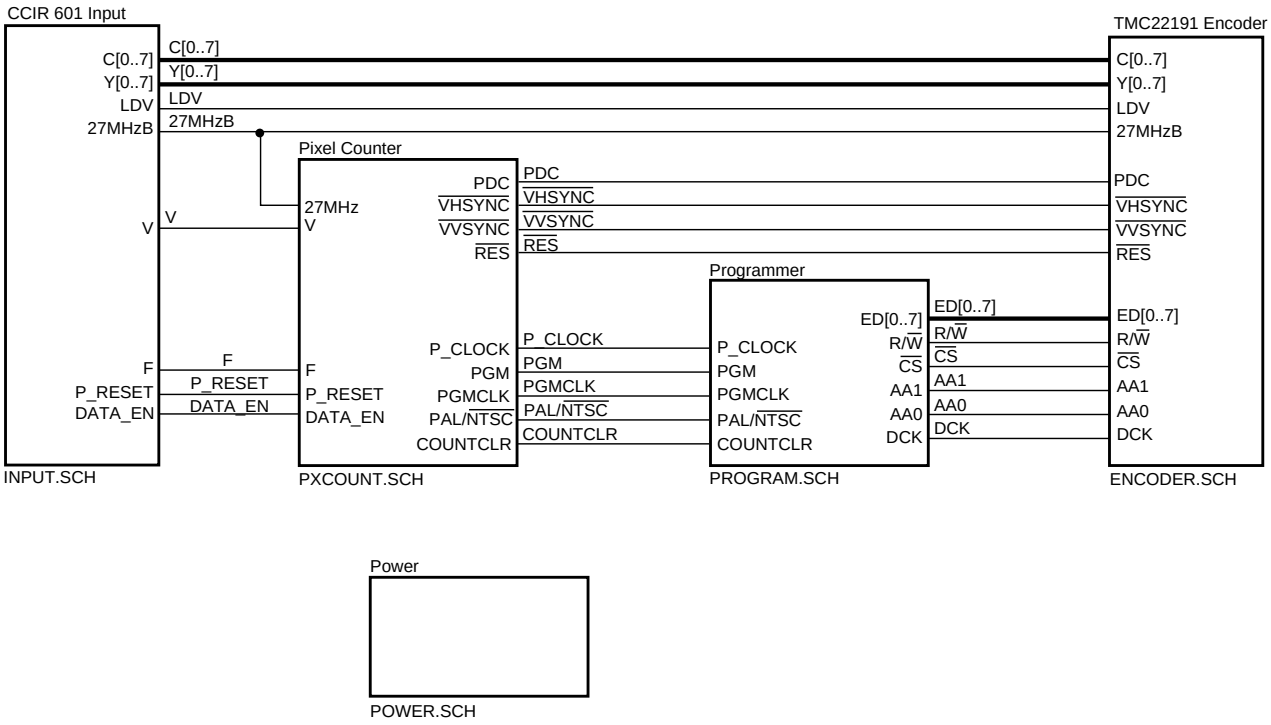
Code Segment 3. TMC22091 Programming Control

```
Board Reference Designator U11
Module  bd1_u11
Title   'TMC22091 programming control'
Declarations
       bd1_u11 device "P20R8';
"inputs"
       clk        pin 1;
       a0,a1,a2,a3,a4,a5,a6         pin 2,3,4,5,6,7,8;
       a7,a8,a9,a10,a11             pin 9,10,11,14,23;
"outputs"
       offset,zero,countclr         pin 22,21,20;
       dck,rw,cs,aa1,aa0            pin 19,18,17,16,15;
"notation"
       addr = [a11..a0];
Equations
       !offset    := ((addr >= 3081) & (addr < 3265));
       !zero      := (addr == 0)
                  # ((addr >= 3264) & (addr <= 3327));
       countclr   := (addr >= 3265);
       !dck       := !a1 & zero;
       !rw        := zero & (addr <= 3261);
       !cs        := (a1 & a0)
                  # (!a1 & !a0)
                  # (addr >= 3263)
                  # !zero;
       !aa1       := (addr <= 9)
                  # ((addr >= 3082) & (addr <= 3085))
                  # !zero;
       !aa0       := !offset
                  # (addr >= 3264)
                  # !zero;
End    bd1_u9
```

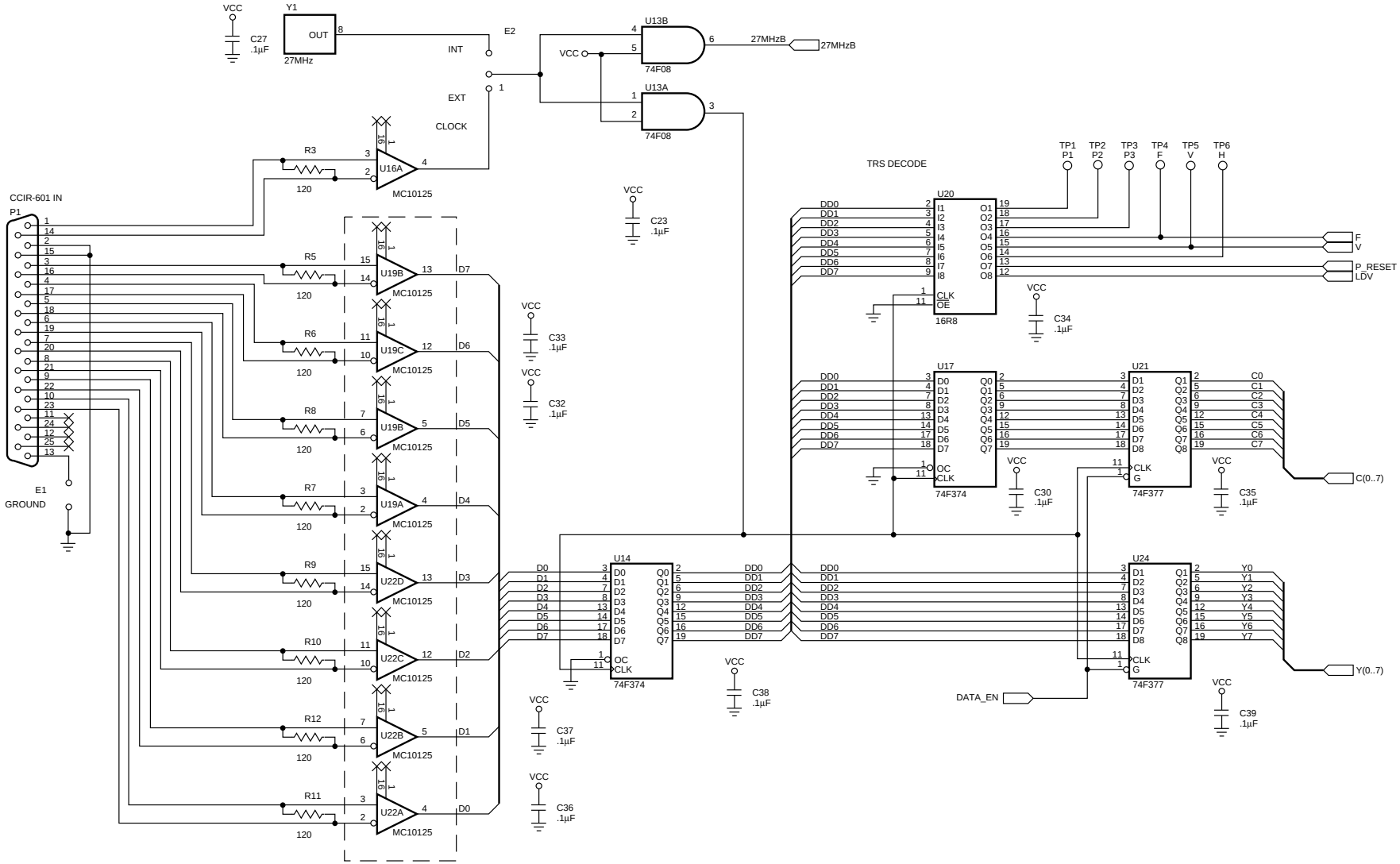
Code Segment 4. TRS Decode

```
Board Reference Designator U20
Module  bd1_u20
Title   'TRS decode'
Declarations
       bd1_u20 device "P16R8';
"inputs"
       d0,d1,d2,d3,d4,d5,d6,d7      pin 2,3,4,5,6,7,8,9;
"outputs"
       p1,p2,p3,f,v,h               pin 19,18,17,16,15,14;
       p_reset,ldv                  pin 13,12;
"notation"
       data = [d7..d0];
Equations
       !p1         := (data == ^hFF);
       !p2         := (data == ^h00) & !p1;
       !p3         := (data == ^h00) & !p2;
       !h          := (!h & p3) # (!d4 & !p3);
       !v          := (!v & p3) # (!d5 & !p3 & !d4)
                   # (!v & !p3 & d4);
       !f          := (!f & p3) # (!d6 & !p3 & !d4)
                   # (!f & !p3 & d4);
       !p_reset    := !p3 & d4;
       !ldv        := !p_reset # ldv;
End    bd1_u9
```

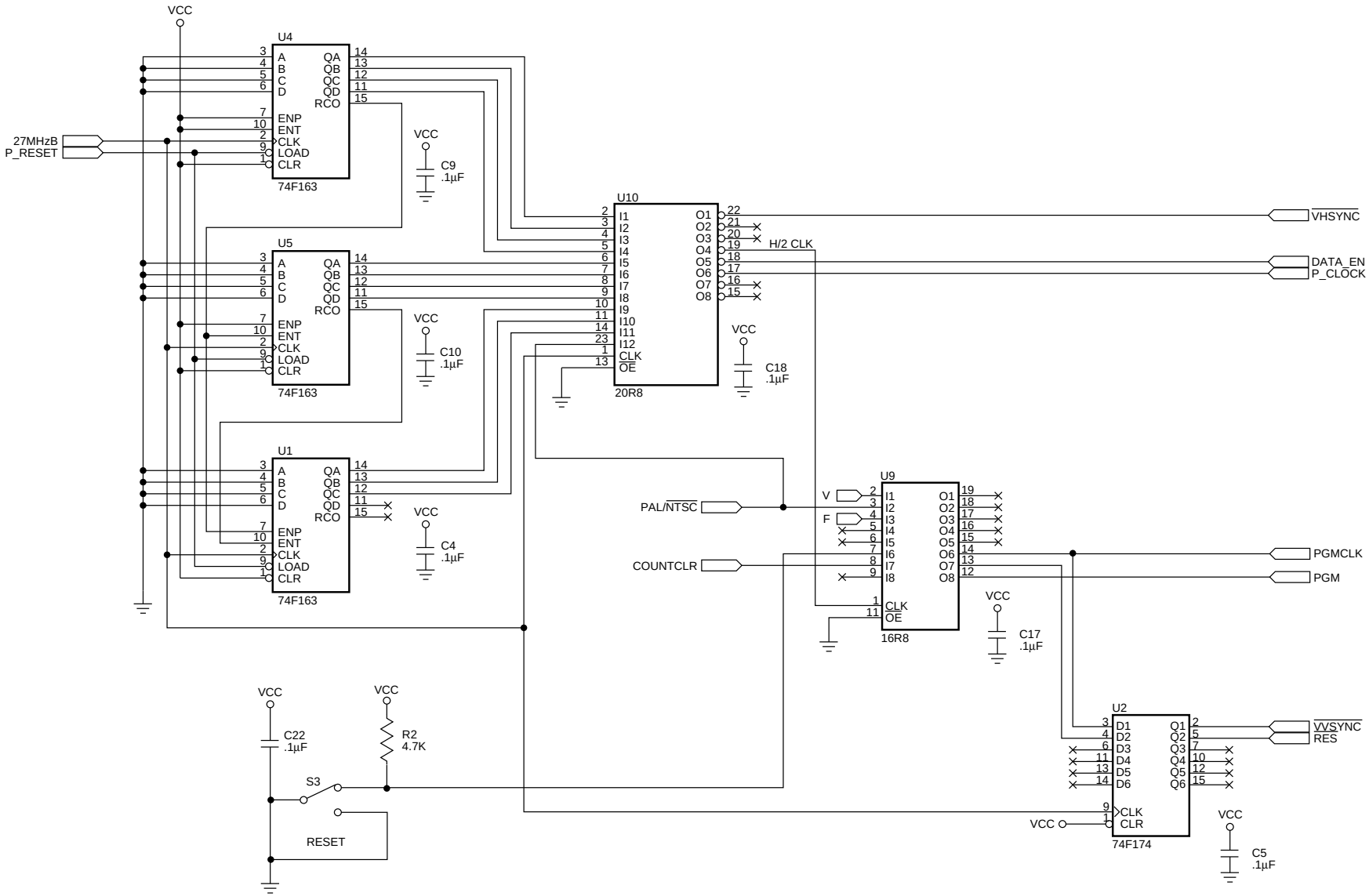
Digital Video Encoder Demonstration Board



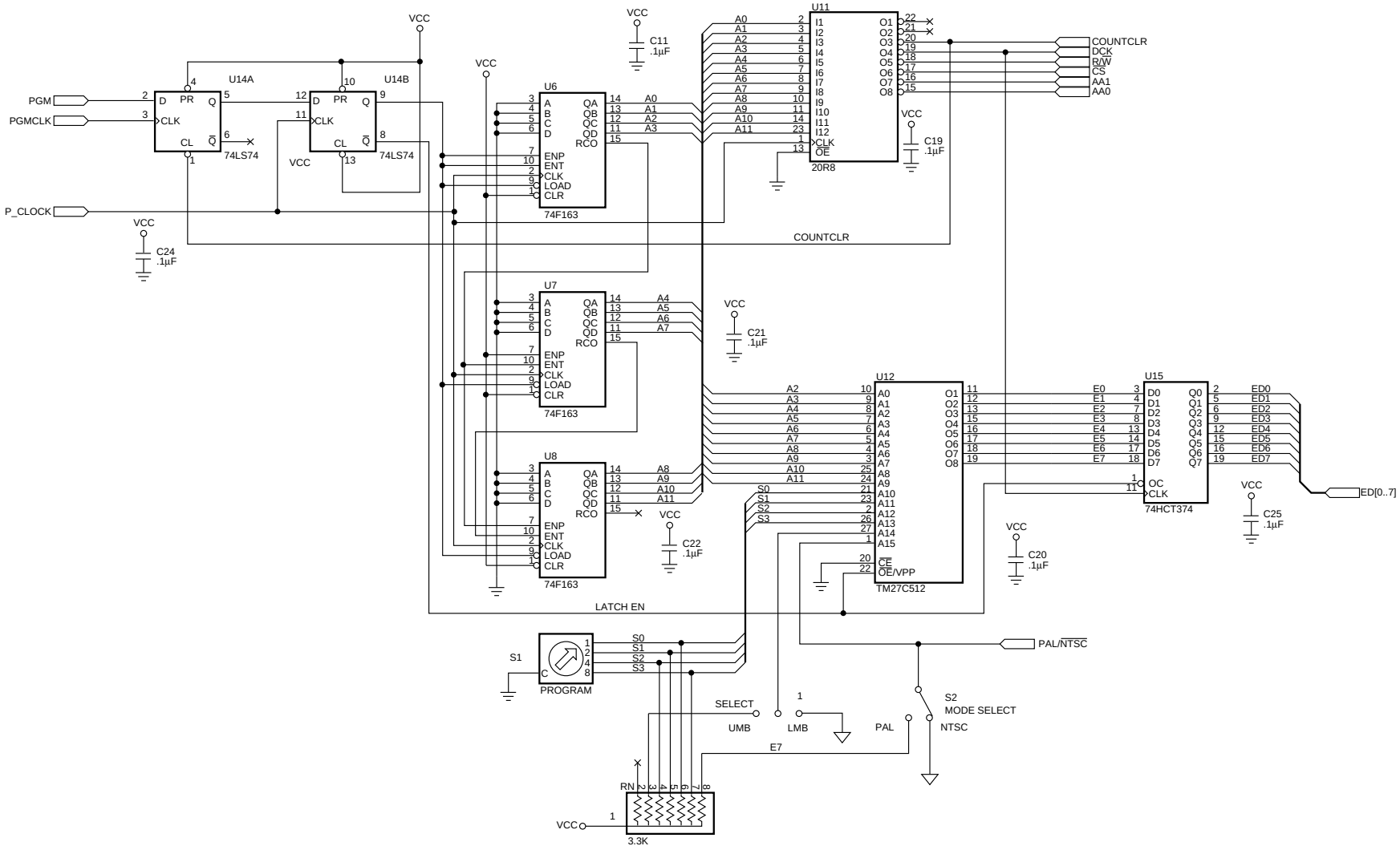
Digital Video Encoder Demonstration Board



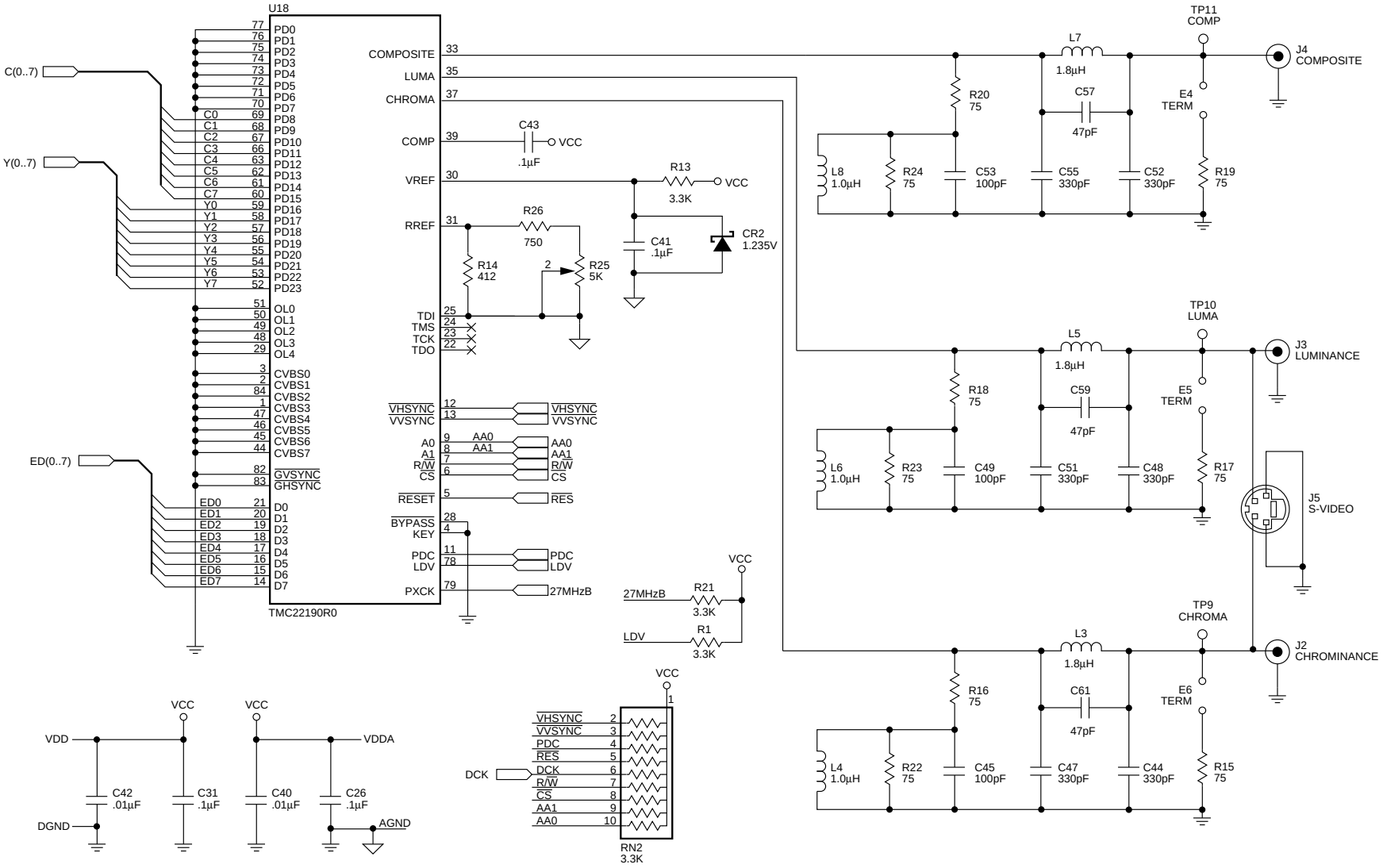
Digital Video Encoder Demonstration Board



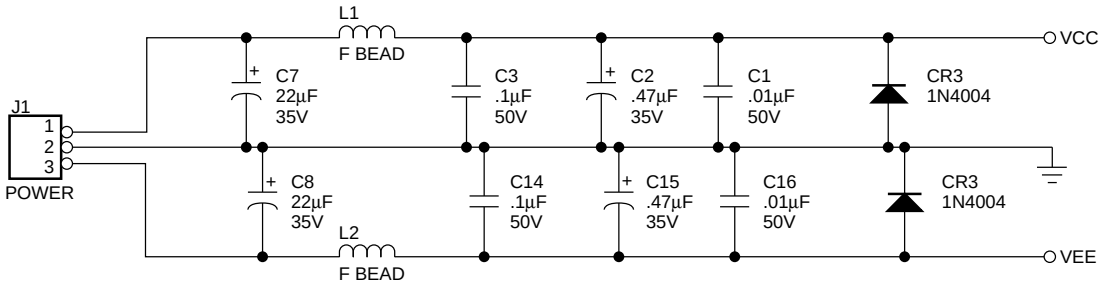
Digital Video Encoder Demonstration Board

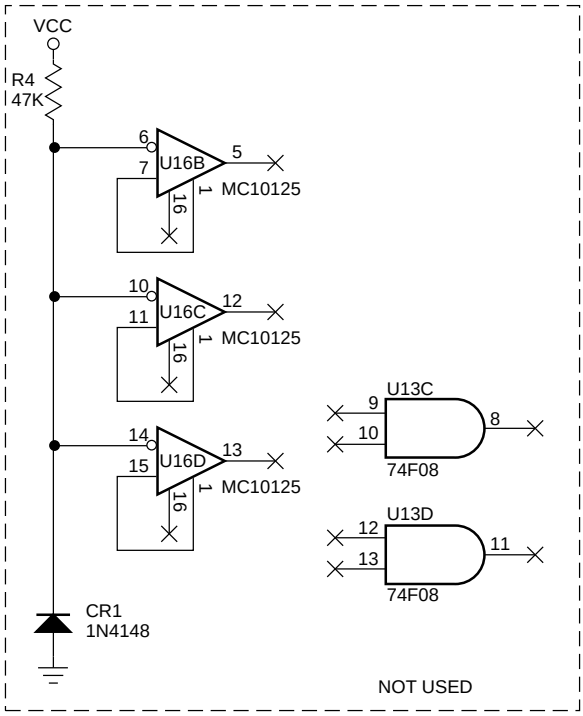


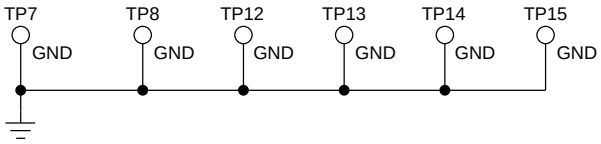
Digital Video Encoder Demonstration Board



Digital Video Encoder Demonstration Board







Ordering Information

Product Number	Temperature Range	Speed Grade	Screening	Package	Package Marking
TMC22061P7C	25°C	27 MHz	Commercial	5" by 9" PCB	TMC22061P7C

A schematic database is available in OrCAD™ format, along with PAL and EPROM maps. Contact the factory.

The TMC22061 Demonstration Board, design documentation, and software are provided as a design example for the customers of Raytheon. Raytheon makes no warranties, express, statutory, or implied regarding merchantability or fitness for a particular purpose.

All parameters contained in this specification are guaranteed by design, characterization, sample testing or 100% testing as appropriate. Raytheon reserves the right to change products and specifications without notice. This information does not convey any license under patent rights of Raytheon Company or others.

Raytheon Electronics
Semiconductor Division
5580 Morehouse Drive
San Diego, CA 92121
619.457.1000
800.722.7074
Fax 619.455.6314
applications@lj.sd.ray.com